ARINC 429 IP-Core with DO-254 Package

Multi-target, Flexible and Customizable

ARINC 429 library for integration into your design as a source code, configured according to your specifications, and delivered with its own DO-254 documentation package for certification.

Key Features and Benefits

Applicable Standards:

- Supports ARINC 429 standard part 1, 2 and 3
- Developed according to RTCA/DO-254 ED-80 guidance (DAL-A to DAL-D criteria)

Configuration support per channel:

- Low speed (LS, 12.5 kHz) or high speed (HS, 100 kHz) mode
- Disable/Enable
- Programmable Overflow, Parity, Frame error bits
- Programmable interrupts on Rx and Tx
- Configurable memory for Labels management

Supported tools:

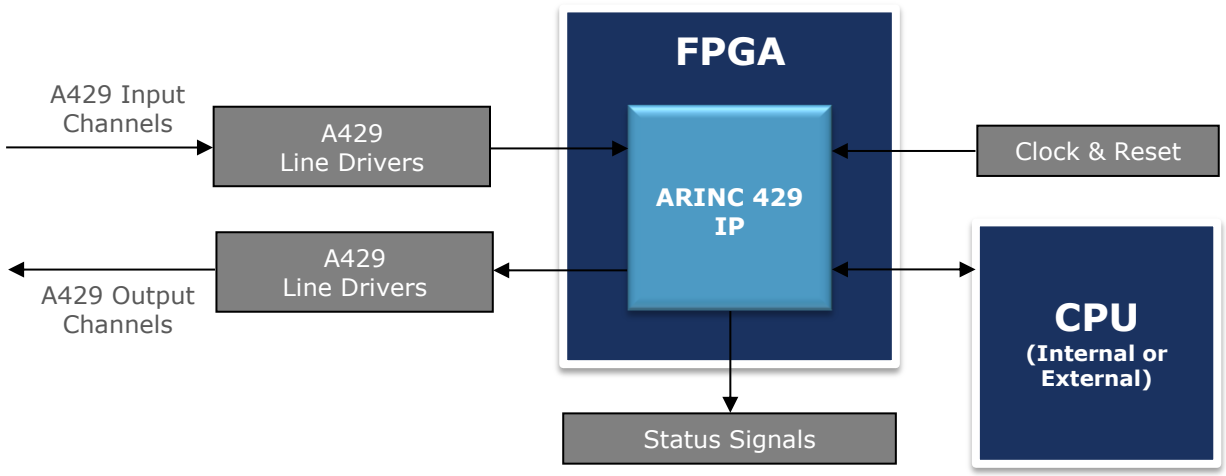
- Xilinx ISE & Vivado
- Microsemi Libero
- Altera Quartus
- Mentor Graphics ModelSim, Questa
- Cadence
- Synopsys Synplify

Technical features:

- Supported CPU interfaces: AMBA AXI4Lite, Avalon, asynch. or customizable interface
- Flexible architecture allowing from 1 Rx and 1 Tx to unlimited number of Rx and Tx
- Independent channel configuration via the CPU interface
- 63 word buffer (FIFO) for each ARINC 429 input channel
- 31 word buffer (FIFO) for each ARINC 429 output channel
- Provided with a full-automated test bench with 100% code coverage

Available Platforms:

- Microsemi FPGA & SoC
- Altera FPGA & SoC
- Xilinx FPGA & SoC
- ASIC technology



General description

The ARINC-429 IP Core is a multi-channel ARINC 429 transmitter and receiver core for serial communication in airborne applications. The IP is developed, validated & licensed by Oxytronic.

This IP Core has been developed according to the RTCA/DO-254 ED-80 guidelines. These guidelines are required by the Airworthiness Certification Authorities (EASA and FAA) for hardware developments that need to be certified for the use in commercial aircraft equipment.

The IP Core incorporates various state-of-the-art CPU interfaces which can easily be connected to your required interface. Each individual channel can be configured according to your specifications.

Each channel contains a specific buffer (FIFO), incorporated in the IP. This allows efficient data transfer between CPU and the IP.

Documentation and Data items

Basic deliverables

- Datasheet
- IP ARINC-429 Netlist
- Functional verification test bench obtaining 100% code coverage
- Simulation and implementation scripts and logs in order to regenerate the same functional behavior
- Implementation results

Deliverables for RTCA/DO-254 certification

- VHDL RTL sources compliant to the Oxytronic coding standard
- Delivered Documents (part of the IP package deliverables):

  Certification Liaison Process
  - Plan for Hardware Aspect of Certification (PHAC)
  - Hardware Accomplishment Summary

  Hardware Planning Process
  - Hardware Development Plan
  - Hardware Validation and Verification Plan (HVVP)
  - Configuration Management Plan
  - Hardware Process Assurance Plan

  Hardware Development Process
  - Requirements capture
  - Conceptual design data
  - Detailed design data

  Hardware Verification and Validation Process
  - Traceability Matrices
  - Hardware Verification Procedures
  - Verification Reports

  Hardware Configuration Management Process
  - Hardware Configuration Index
  - Hardware Environment Configuration Index

  Hardware Process Assurance Process
  - Audit report
  - Records

- Available Documents (for audit purpose only, not part of the IP package deliverables):

  Hardware Verification and Validation Process
  - All reviews, audits and corresponding checklists

Implementation Data

Device	Description	System Clock	Needed Resources
Microsemi PROAsic3 A3P015	- 32 Rx channels - 16 Tx channels - CPU interface	50 MHz	- 20199 core cells - 20 memory blocks
Microsemi PROAsic3 A3P015	- 1 Rx channels - 1 Tx channels - CPU interface	50 MHz	- 1189 core cells - 4 memory blocks
Microsemi Igloo2 M2GL050T	- 32 Rx channels - 16 Tx channels - CPU interface	50 MHz	- 8137 LUTs / 7886 SLEs - 20 memory blocks
Microsemi Igloo2 M2GL050T	- 1 Rx channels - 1 Tx channels - CPU interface	50 MHz	- 580 LUTs / 492 SLEs - 4 memory blocks
Microsemi SmartFusion2 M2S050T	- 32 Rx channels - 16 Tx channels - CPU interface	50 MHz	- 8137 LUTs / 7886 SLEs - 20 memory blocks
Microsemi SmartFusion2 M2S050T	- 1 Rx channels - 1 Tx channels - CPU interface	50 MHz	- 580 LUTs / 492 SLEs - 4 memory blocks
Altera Cyclone V 5CEBA2	- 32 Rx channels - 16 Tx channels - CPU interface	50MHz	- 4244 ALMs - 10 memory blocks
Altera Cyclone V 5CEBA2	- 1 Rx channels - 1 Tx channels - CPU interface	50MHz	- 259 ALMs - 2 memory blocks
Altera Arria10 10AS016E3	- 32 Rx channels - 16 Tx channels - CPU interface	50MHz	- 4251 ALMs - 10 memory blocks
Altera Arria10 10AS016E3	- 1 Rx channels - 1 Tx channels - CPU interface	50MHz	- 259 ALMs - 2 memory blocks
Xilinx Spartan 6 xc6slx75	- 32 Rx channels - 16 Tx channels - CPU interface	50 MHz	- 8162 LUTs/Registers - 10 memory blocs
Xilinx Spartan 6 xc6slx4	- 1 Rx channels - 1 Tx channels - CPU interface	50 MHz	- 471 LUTs/Registers - 2 memory blocs

Device	Description	System Clock	Needed Resources
Xilinx Artix7 XC7A15T	- 32 Rx channels - 16 Tx channels - CPU interface	50 MHz	- 7727 LUTs/Registers - 10 memory blocs
Xilinx Artix7 XC7A15T	- 1 Rx channels - 1 Tx channels - CPU interface	50 MHz	- 461 LUTs/Registers - 2 memory blocs
Xilinx Kintex7 XC7K70T	- 32 Rx channels - 16 Tx channels - CPU interface	50 MHz	- 8051 LUTs/Registers - 10 memory blocs
Xilinx Kintex7 XC7K70T	- 1 Rx channels - 1 Tx channels - CPU interface	50 MHz	- 493 LUTs/Registers - 2 memory blocs

Contact us for more configuration samples

Service Experience

Several releases of our ARINC-429 IP Core have been successfully integrated into several FPGA for use in equipment that have been certified by FAA and EASA (DAL-A and DAL-B).

Business Model

Oxytronic proposes a flexible business model adapted to clients' needs and context, with associated design services for any turnkey adaptations.

To ensure certification of your product, Oxytronic delivers an IP tuned to your specification needs. Adjustable features such as number of receiver or transmitter channels, labels, etc… are taken into account into the RTL code and in the DO254 document package as well.

Oxytronic also offers evaluation of the IP on demand.

Oxytronic overview

Oxytronic is an electronics equipment design and production company, located in France.

Oxytronic provides:

- standard equipment for In-Flight Entertainment and Cabin Management Systems,
- design services for safety-critical applications (DO-254),
- custom electronics design services & manufacturing (FPGA, boards, systems, and full equipment development) for the Aerospace and Defense industry.

With the acquisition of Barco Silex France early 2017, Oxytronic now provides safety-critical equipment development according to RTCA DO-254 / Eurocae ED-80, from conception to certification support, up to DAL-A.

More information

For additional information about Oxytronic products and design services, please *Contact us*

www.oxytronic.fr