# Safety-Critical FPGA

# AVP254 - Automatic Verification Platform for FPGA

## The Smart Solution for FPGA Physical Testing !

**Oxytronic AVP254 is an automatic physical verification platform for FPGA, especially developed to meet safety-critical FPGA verification objectives, while drastically saving testing costs and delays.**

## Benefits

**Accelerate your Time-to-Market and save money**

- Reuse your RTL simulation patterns for FPGA physical verification without redeveloping test vectors
- Reuse your generic testbench for the verification of next FPGAs

**Provide comprehensive test coverage rate on target board**

## Key Features

**Physical verification environment base, with associated virtual simulation model**

- FPGA on board and FPGA virtual verification for all FPGA vendors
- One single set of procedures for both environments

**Fully automatic and self-checking testbench**

- Requirements based log files and associated status
- Detailed measurements values and code coverage metrics reports

**Includes standard set of qualified functions**

- Basic signal acquisition and generation operations
- Loop management for recurring sequences

**Easy integration of user defined functions**

- Client-specific interfaces management capability: ARINC, AFDX, CAN, 1553, PCIe…
- Third-party models integration

**Device Under Test power supply management**

- Customisable power supplies
- Automatic power management to prevent hardware damages during tests

**Reusable and based on industry standard**

- Solution based on NI PXI architecture
- Generation of ASCII log files for external processing
- Easy migration to production tests

**DO254 flow compliance**

- Many successful certifications for our customers up to DAL A by both FAA and EASA authorities
- Support up to SOI#4

## More Information


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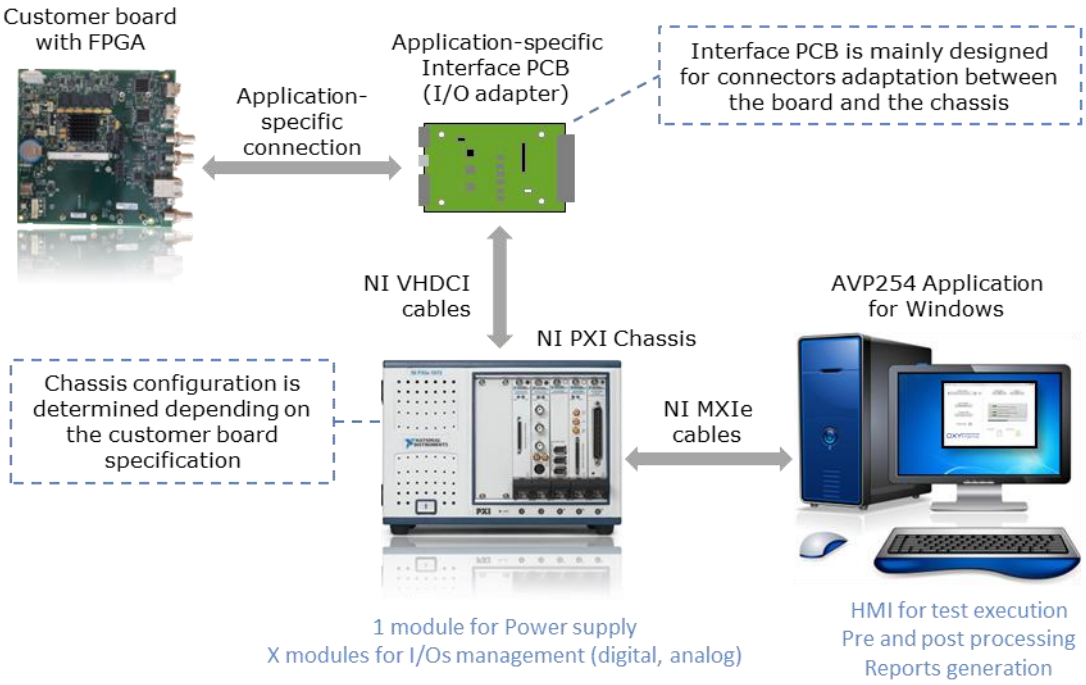
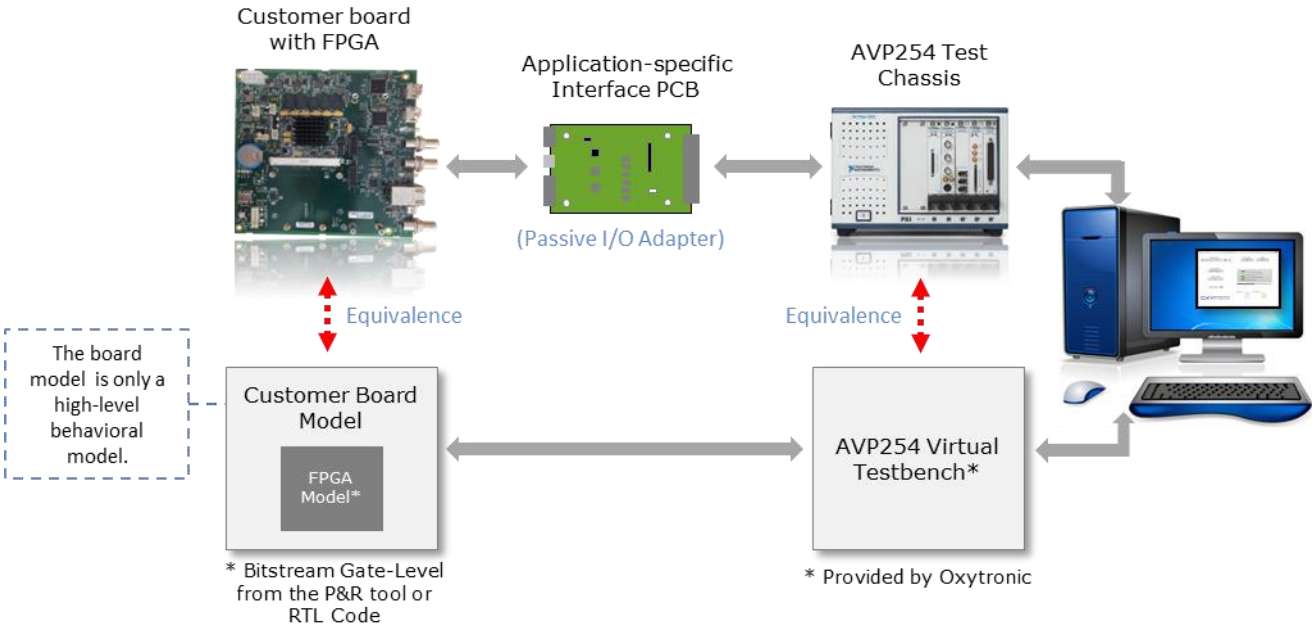
## Hardware Architecture

Based on the customer board specification, Oxytronic defines the best hardware solution for the physical verification, including: chassis, modules, cables and specific PCB. Then we develop the testbench setup to provide a ready-to-use automatic solution for the Client.




## Virtual Simulation and Physical Verification Equivalence



## Power and IOs management

**Device Under Test power supply:**
- Configurable number of sources
- Configurable voltage range for each source
- Soft controlled to prevent hardware damages

**Digital IOs management:**
- Sampling frequency up to 200 MHz
- Configurable voltages

**Analog IOs management:**
- Customisable features : sampling frequency, voltage range and accuracy

## Qualified Standard Function Set

**ASSIGN**
Assign a value to a single signal or to a bus

**SET_IO_DIR**
Define the direction of the IO lines

**CHECKOUT**
Check the value of a signal

**CHECKSIG**
Check the period and the duty cycle of a signal

**CHECKTIME**
Check the time between two events

**WAIT_EVENT**
Wait for an event on a signal

**WAIT_TIME**
Wait for a defined time

**LOOP / LOOPx**
Repeat a sequence of instructions

**DISPLAY**
Display a message in the log file

## User-defined Function Set

**SET_COM**
Give the configuration and the data to be sent using user defined interfaces

**CALCULATE**
Call the user defined algorithm models

**GET_COM**
Check configuration and data received using user defined interfaces

## Implementing Communication Protocols (AFDX, ARINC, CAN, PCIe…)

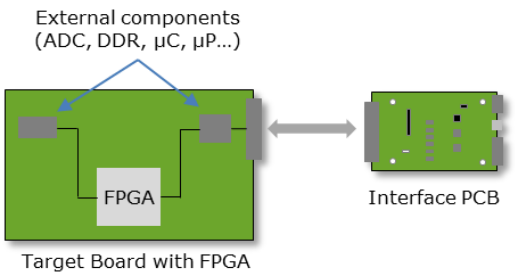
When the target board implements a communication protocol, the protocol has to be implemented at hardware and software level in the testbench. Oxytronic provides the best optimized solution in terms of cost and performances:

- either by choosing a dedicated PXI module, or a combination of free IOs and HW components on the interface PCB to implement the protocol
- either by writing the communication function using the User-defined function set, or by implementing an existing third-party IP.
- and by providing the qualification report for the function

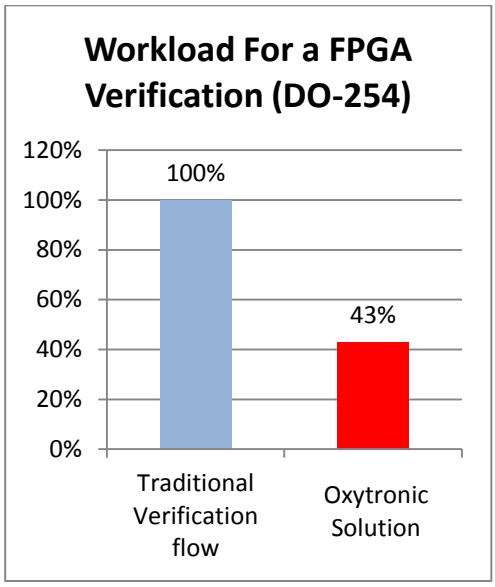
## Implementing external components (DDR, µP, µC, ADC…)

AVP254 is also able to verify requirements implemented in the FPGA through external components on the board like external memories, microcontrollers/processors, ADC…

At the virtual simulation level, Oxytronic will develop a model of each external component. A model does not need to represent all functionalities of the component: it is only a VHDL/C high-level behavioral model.



## Comparison between traditional verification and the Oxytronic solution




### Real Facts

This illustration shows the verification workload for an FPGA that uses a traditional verification methodology (test vectors are written for the simulation, and then re-written for the physical verification) compared to the workload using our automatic testbench.

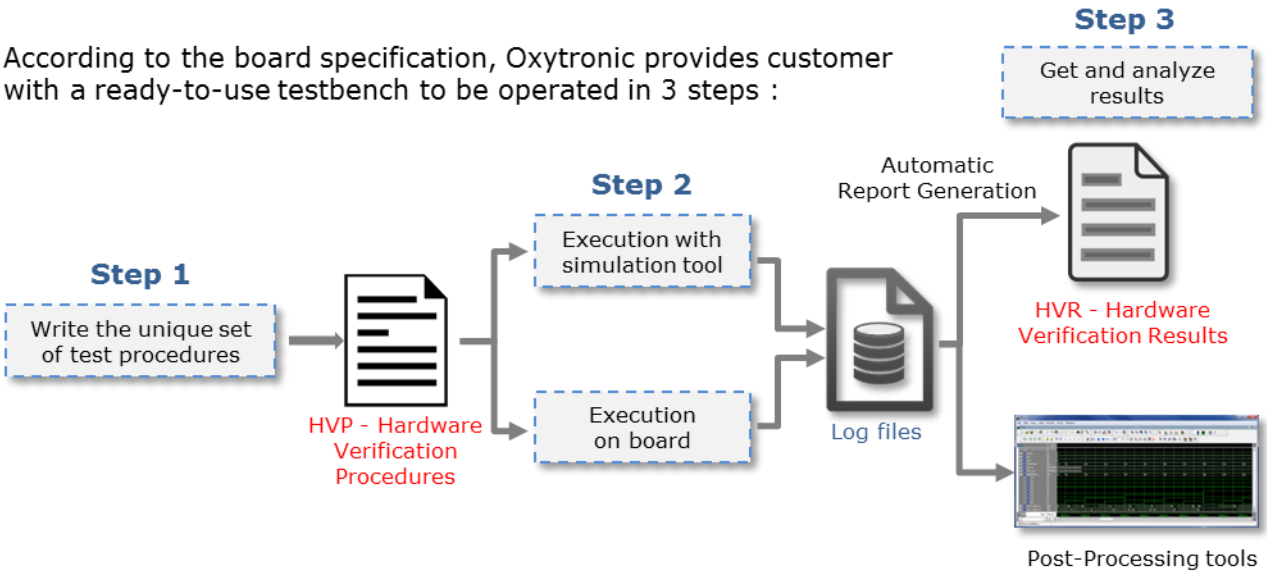
Results examples are related to a real project developed by Oxytronic with following characteristics :

- FPGA : Microsemi A3PE3000, 83% full
- Nb of I/Os : 123
- DO-254 Level-A

Using a workload basis of 100% with the traditional methodology, we obtain 43% by using our automatic testbench (including all extra-work necessary for the testbench setup). The gain in terms of work weeks is more than 50%.
The more complex the FPGA is, the higher are the savings.

## Three steps to facilitate your FPGA verification

According to the board specification, Oxytronic provides customer with a ready-to-use testbench to be operated in 3 steps :




## Oxytronic Product Package and Services

**Our offering includes:**

- The full PXI testbench with associated calibration reports, documentation and software including : test sequencer, auto-verification engine, report generation engine and GUI,
- The testbench simulation model,
- A DO-254 qualification report for all native functions,
- A testing PC,
- The design of the specific hardware interface board,
- A training for methodology understanding and platform handling,
- Additional services for the development of your verification functions: custom interfaces development and integration, DO-254 qualification report for all custom functions with associated reviews.