DO-254: Preconceived ideas about
FPGA on-board verification

Idea #1

This series of articles "Preconceived ideas about..." aims at sharing our feedback about specific issues we faced at Oxytronic during various FPGA developments following the DO-254 guidelines. And especially how we solved them and achieved the highest level of verification quality.

DO-254 - "FPGA on-board verification is useless." Are you sure?

RTL and back annotated gate level simulations, Static Timing Analysis, Equivalence checking, clock domains crossing analysis etc… All these verification techniques provide a deep quantified analysis of FPGAs behavior ensuring they conform to their specification requirements.

Thus when the bitstream of the FPGA is loaded on the final application board - after weeks or months of virtual verification – no one can expect a bug to be found at this stage.

So why does RTCA DO254 (§6.3.1) ask for on-board verification of FPGAs in their intended hardware?

Because FPGA modelling libraries can contain bugs.

Virtual verification tools are based on libraries modeling the FPGA logic cells. Even if these libraries have been used in a huge number of designs, they can still contain bugs. We have already found a bug in a memory model leading to incorrect behavior of the FPGA during a simulation, after hours and hours of investigation. So it is necessary to give proof that these libraries are bug free regarding the designed FPGA.

One solution would be to qualify the vendor library. As it is made of hundreds of logic cells it is a very time - and cost - consuming activity.

Another solution is to compare the behavior of the FPGA model running in simulation with an independent verification mean such as a physical board. Thus it ensures the FPGA model used for the virtual verification is correct.

As a consequence, on-board verification ensures that even if there is a bug in the FPGA modelling library it will be detected.

Because FPGA are not only digital components.

Virtual verification tools are working in a full digital world which is well suited for FPGA development. But even if an FPGA is a digital component it remains subject to analogical phenomena: PLL locking time, clock jitter, clock domain crossing, metastability, voltage variations and perturbation …
Just probe two clocks from two different oscillators with an oscilloscope and you will observe a drift between them that you cannot reproduce in a simulator.
In the same way, it is not possible to manage interactions with other components such as power supplies sequencing, reset loops and so on with virtual verification tools.
That shows that testing the FPGA on its final application board often reveals problems linked to those "real life" behaviors.

Because simulations can last a long time.

Who has never complained about an endless simulation?
Virtual verification tools are consuming CPU time which can become huge when the FPGA design contains long duration events (actually starting from a few seconds…). When a bug is found, it has an important impact on the test regression activities so that it is necessary to find a way to cut the verification time. In this case performing tests on the final hardware allows the FPGA to operate at its real speed, so that even if an event occurs after 10 minutes, it will only take 10 minutes to reach on hardware.
This is useful to ensure that the FPGA behavior is correct without having to find artifices such as forcing FPGA internal nodes.
The gain is huge, as shown on the graph below, extracted from a DO-254 project involving a ProAsic3 A3PE3000 Microsemi device 83% full.
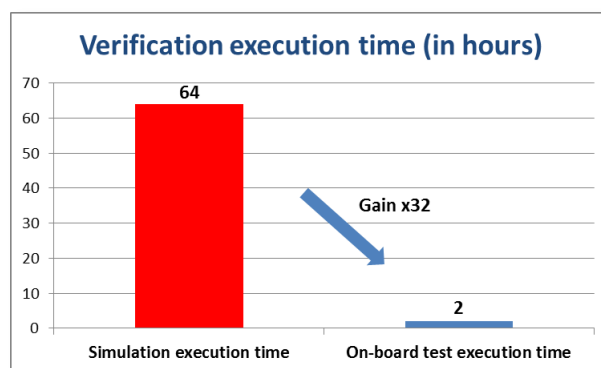
So, on-board hardware verification can be a good way to achieve confidence in the device behavior without running endless simulations.

520 avenue de Jouques
ZI Les Paluds
13400 Aubagne - FRANCE

www.oxytronic.fr

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Is physical verification still useless?

FPGA physical verification on its final application board make it possible to reach long duration events, to address physical phenomena, and most of all to get a high level of confidence in the designed FPGA. Of course through an efficient, automated verification solution.

As a result, do not believe people who say "On-board physical FPGA verification is unnecessary": all these reasons show that FPGA physical verification on its final application board – as required by RTCA DO254 – is not a useless activity.

Francis Raguin is Project Manager at Oxytronic (formerly Barco Silex France). After having successfully lead several DO-254 projects he introduced AVP254 - the DO-254 FPGA verification platform. *For any question, feel free to contact him:*
francis.raguin@oxytronic.fr.

For more information about AVP254, our DO-254 FPGA verification platform: Here