This series of articles "Preconceived ideas about..." aims at sharing our feedback about specific issues we faced at Oxytronic during various FPGA developments following the DO-254 guidelines. And especially how we solved them and achieved the highest level of verification quality.

DO-254 - "FPGA on-board verification needs huge human and material resources." Is this true?

The verification of FPGAs on-board often requires to drive and to monitor a large number of signals either at the board interfaces or directly on some board tests points.
For this reason, when talking about physical verification, people usually have in mind a lot of complex electronic lab tools interfaced with the hardware under test by mean of thousands of cables and driven by a dedicated team of specialists.
On the contrary, at Oxytronic we have experienced solutions that drastically simplify hardware resources and decrease the necessary workforce.

Which hardware material do I need to perform FPGA on-board verification?

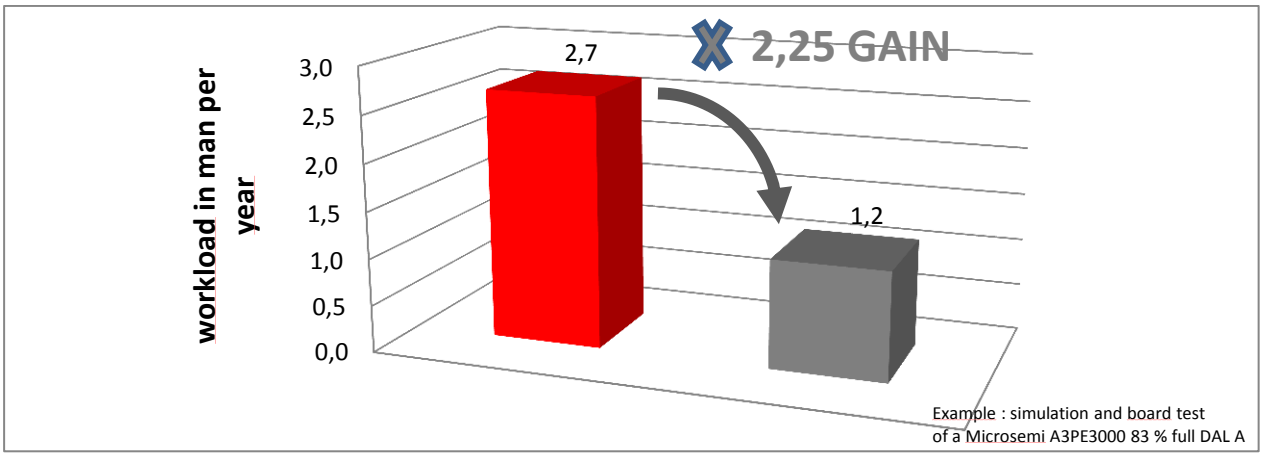
To perform FPGA on-board verification, it is possible to use conventional electronic lab equipment. For instance the stimuli can be generated by wave and pattern generators. But these tools allow only a focus on a specific part of the FPGA behavior. In the same way the response of the device under test can be recorded by using oscilloscopes and logic analyzers but with a limited visibility. Using multiple equipment will also result in a complex test setup due to all different kinds of interconnections with the device under test too, and because it is necessary to synchronize them all together.

What about human resources?

When working with conventional electronic lab equipment, engineers involved in the physical verification activity must be familiar with this kind of hardware. Furthermore, as the manual part remains important for both generating the stimuli and analyzing the results, the need in term of resources is important: it takes a lot of time to write each procedure to be applied because the configuration of all tools must be described; it also takes a lot of time because the configuration of all tools must be applied; and then it takes a lot of time because the results given by the tools (mainly records of chronograms) must be logged and analyzed. In case of regression testing, the manual execution and analysis of the test results must be done again, leading in important need of human resources.

Using the right tools

Another way is to take advantage of modular hardware platforms based on a chassis equipped with configurable modules. At Oxytronic, we experienced the National Instruments PXI solution with LabVIEW. It allows automating the test for both stimuli generation and results analysis with a dedicated and unique test tool. Thus it drastically decreases the necessary workforce to achieve on-board verification. But furthermore, and because this hardware is based on FPGAs, it is possible to model this physical testbench to perform DO254 FPGA simulation. Its gives another mean to decrease the workforce needed by using the same stimuli for both virtual and physical FPGA verification activities. We measured a gain greater than 2 on real projects.



Moreover and thanks to the configurability of such solutions, it is even possible to use the same material for testing various FPGAs for several projects: we realized that we used almost the same kinds of I/O from one project to the other.
For the engineering team, it limits the need of people involved in the physical verification activity, while providing an easy-to–use and reusable verification environment.

Physical verification is complex but…

Due to its complexity, the FPGA on-board verification is challenging regarding to the material and the human resources involved in this activity. Thus, it is important to take care of the testbench architecture because it has a major impact on these two aspects. Using automated, self-checking, reusable test solutions will help limit the pain – and thus the resources – associated to the FPGA physical verification in a DO-254 context.

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For more information about AVP254, our DO-254 FPGA verification platform: Here