This series of articles "Preconceived ideas about..." aims at sharing our feedback about specific issues we faced at Oxytronic during various FPGA developments following the DO-254 guidelines. And especially how we solved them and achieved the highest level of verification quality.

DO-254 - "FPGA on-board verification has a limited value, due to a lack of I/O visibility." Is this true?

One of the major technical concerns when dealing about FPGA on-board verification is the lack of visibility for both FPGA pins and internal nodes. Thus as the DO-254 asks for physical verification of FPGAs in their intended environment, we usually have in mind that it will be impossible to have enough visibility on I/O pins in order to fully cover the requirements by mean of hardware testing.
But what are the different ways for testing a FPGA directly on its target board? Which visibility can we really and objectively expect and how does it fit with the DO-254 constraints?

Internal node level observation

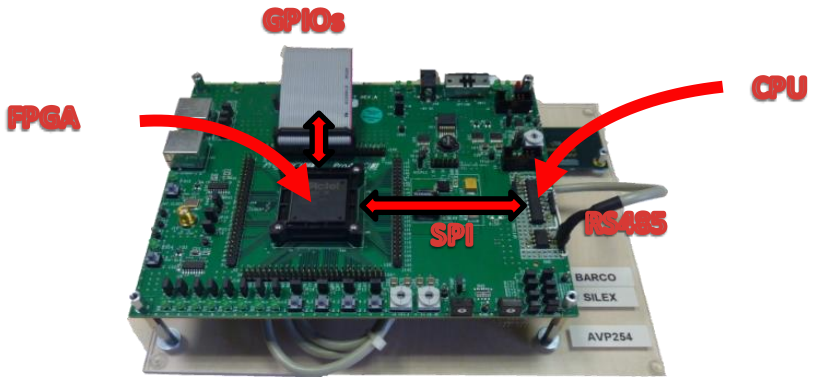
Internal node level observation gives the highest level of detail during verification and is provided by the FPGA vendors because they all purpose to embed a small logic analyzer into their components. Thus, thanks to a JTAG probe connected to the FPGA, you can monitor the internal nodes of the device. Unfortunately most of the time this solution requires to modify the FPGA bitfile and it can lead to some difficulties regarding to the certification authorities. Another way to proceed is to make internal nodes visible through FPGA pins (for example using a serial link dedicated to internal node monitoring) but then you will have associating requirements to these functions in your FPGA specification and you will waste some logic to do this.

I/O pins level observation

I/O pins level observation allows the test of the FPGA as a black box. To get access to all FPGA I/O pins, one solution consists in isolating the FPGA (for example by using a semiconductor tester) and then applying the stimuli extracted from the simulation stage. This solution has two main drawbacks: the first one is that you should have performed the virtual verification before starting the physical one, the second one is that it does not fulfill DO-254 expectation which asks to test the FPGA on its intended environment.

Take advantage of your hardware!

Another way to access FPGA I/Os is to take advantage of its application board. Even if all FPGA I/O pins are not accessible on the interface connectors of the board, it is still possible to have access to them. For example a CPU connected to the FPGA to be tested can be reprogrammed to become a part of the FPGA testbench. Then you will get accessibility to FPGA I/Os thanks to the CPU. That was successfully done and approved by certification authorities in one Oxytronic project.



In the same way, when the board contains components such ADCs or DACs, it is possible to use them as a part of the testbench. In this case, the physical testbench must manage analog I/Os while the virtual testbench modelizes the behavior of the analog component of the board.
The main advantage here is that it is totally in line with the DO-254 expectation as the component is tested in its intended environment.
So it is possible to get access to FPGA I/Os even on its final application board, by reallocating the components around the FPGA to integrate them into the testbench.

Physical verification: I/Os are still visible

Testing a FPGA on hardware can be done by several ways. However, due to DO-254 expectations, it is necessary to make the verification on the final application board, and without modifying the FPGA bitstream with specific code not described in its specification. A deep study of the board architecture allows using the components around the FPGA as part of the testbench, and then getting visibility on the I/Os.

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For more information about AVP254, our DO-254 FPGA verification platform: Here