Porting the Simulation Environment of an Avionics FPGA Component (DO-254 DAL-A) to a Physical Verification Test Bench

The Challenge

Performing the physical verification of an FPGA device by reusing its virtual simulation environment, following a DO-254 Level A methodology flow (Guidance document for the development of hardware components for airborne equipment).

The Solution

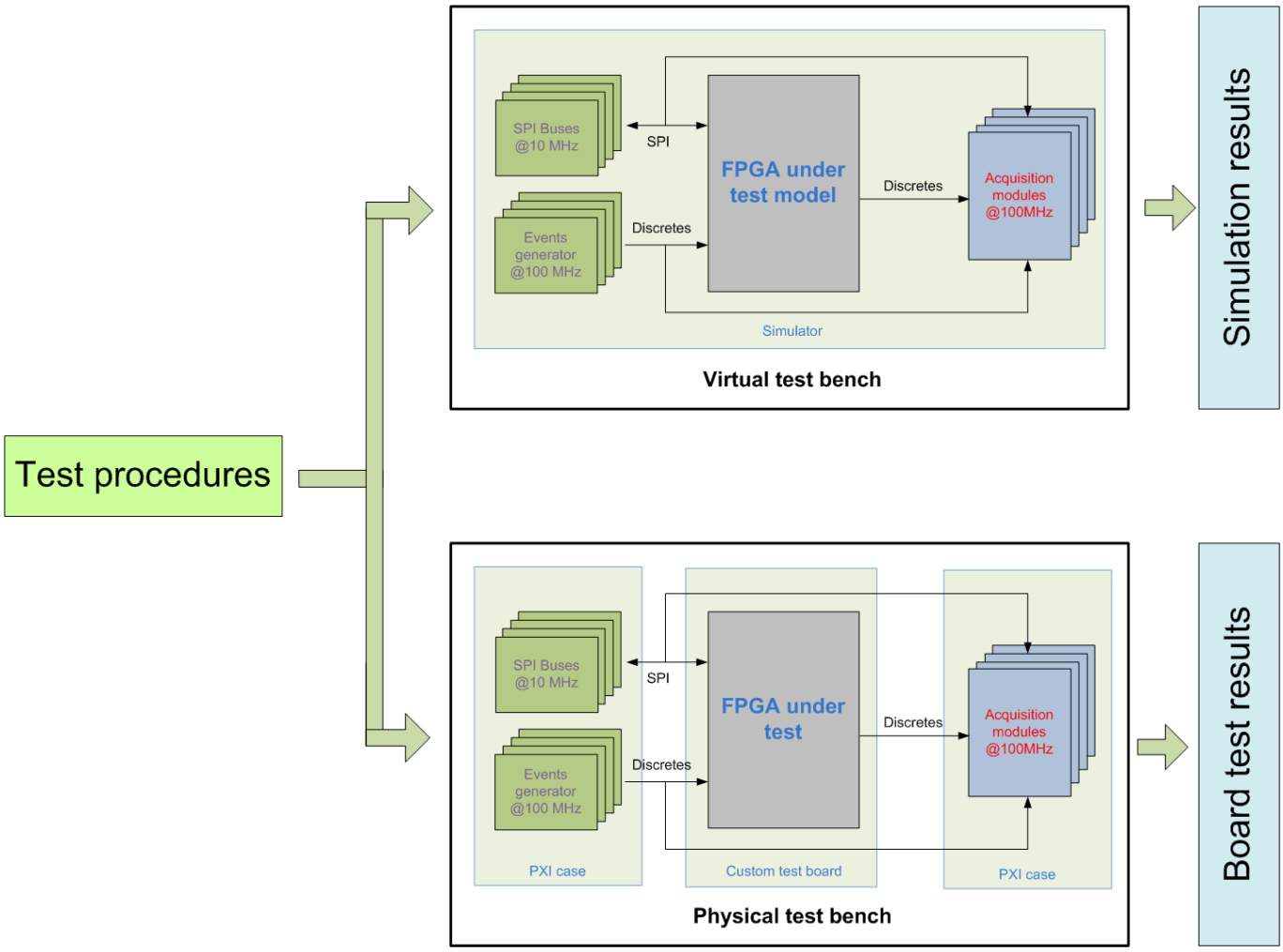
- Designing a test system using an NI PXIe-1073 chassis with two NI PXIe-7962R FlexRIO boards coupled with two NI 6581 modules sharing the characteristics of the simulation environment of the component under verification
- Programming the FPGA chips of the FlexRIO boards using the LabVIEW FPGA Module to integrate the constitutive elements of the virtual test bench
- Handling data exchanges with the PXI equipment and generate the set of test patterns and associated result sheets.

The NI test set consists of a PXI-1073 chassis with two PXIe-7962R modules combined with two NI 6581 adapters. With an acquisition frequency up to 100 MHz, they allow monitoring of various FPGA input and output signals.

The usual approach to verify electronic components and ensure proper functional behavior is to use simulation tools. This type of verification allows testing an FPGA from its Register-Transfer Level (RTL) representation as well as at the logic-gate level by incorporating the timing and gate delay notions.

The verification is then based on timing models of the constitutive elements of an FPGA (logic gates, PLL, memories, and so on).

However, the device behavior must also be silicon proven to meet the DO-254 Level A expectations. Therefore, we developed a test bench based on NI equipment and a custom Printed Circuit Board (PCB) to replicate the virtual verification environment at the physical level, while taking advantage of existing simulations.



The virtual test bench and the physical test bench both allow the same inputs and generate the same type of output data. The test procedures can hence be written for both.

A Unique Test Procedure

Using Perl-based software, the virtual test bench decodes the test procedures described by means of instructions to control both a test engine and the interfaces of the component to verify. LabVIEW can call this Perl program and allows the use of the same test vectors as those used on the virtual test bench. Therefore, the procedures set made and validated for FPGA simulations can be used directly on the physical test bench.

A Shared Architecture

The test engine architecture we developed and validated, as well as the interfaces of the component under verification, are written in VHDL language and can be interpreted by the simulator. The specification and design of this test environment are constrained by the portability between the simulator and the NI framework.

The FlexRIO boards can therefore use this VHDL code to produce a physical test environment identical to the virtual one. Thanks to LabVIEW FPGA, we were able to integrate this code without any change while adding the necessary interfaces to handle the data exchange between the PXI bus and test PC.

Flexible Tools

In this way, we could combine three kinds of hardware description of the FlexRIO boards:

- the use of IP integrated inside LabVIEW FPGA,
- the VHDL code generation from the GUI of LabVIEW FPGA,
- the integration of the VHDL code complying with our quality standards. It allows the user to make the best out of each of these three solutions and integrate all of them into the same environment.

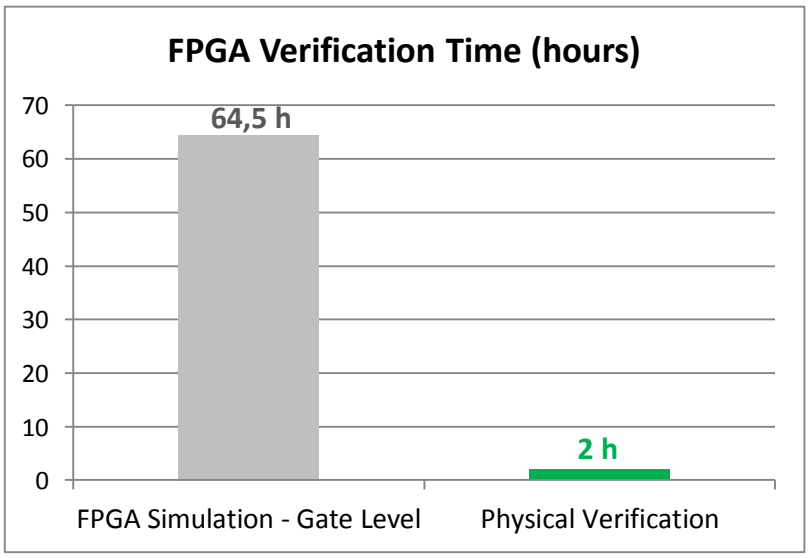
Easier Development

With the reference designs for the LabVIEW FPGA IP cores, we were able to quickly develop data exchange mechanisms via the PXI bus. Besides that, the specific part of the VHDL code we designed had already been validated with the virtual test environment.

We were able to integrate the various hardware and software elements by adding software monitoring probes throughout the processing chain, that is, in the FlexRIO FPGA boards and in the LabVIEW program.

Exact Compliance with the DO-254 Requirements and Time Saving

The physical test bench offers the same functionalities as the virtual test bench, that is, signal generation and acquisition at a frequency of 100 MHz, while delivering test results 30 times faster than the simulator.



Execution of all the FPGA verification procedures: 64.5 hours via logic gate level simulations VS 2 hours via physical tests. The time saved is around a factor of 30.

Additionally, because the two environments are identical, the code coverage score obtained in the virtual simulation reflects also the coverage achieved on silicon during the physical verification. It is therefore possible to provide metrics demonstrating the completeness of the verification on board.

Finally, our solution has been successfully certified (SOI#4) by FAA and EASA authorities for six airborne programs.

About Oxytronic

Oxytronic is an electronics equipment design and manufacturing company for the Aerospace, Defense, Nuclear and Industry area. With the acquisition of Barco Silex France in 2017, we now have a strong expertise and over 10 years of experience in ASIC and FPGA development under DO-254 guidance for prestigious clients such as Airbus, Safran, Thales, etc.

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